

In the Claims

1 1. (Original) A phase-locked loop bandwidth calibration circuit, comprising:
2 a programmable charge pump;
3 a phase-locked loop filter operatively connected to said programmable charge pump;
4 an oscillator, operatively connected to said phase-locked loop filter, to generate a
5 frequency signal based upon a signal received from said phase-locked loop filter; and
6 a control loop operatively connected to said phase-locked loop filter and said
7 programmable charge pump;
8 said control loop controlling said programmable charge pump to adjust its output current
9 level based on a measured gain of said oscillator.

1 2. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 1,
2 wherein said control loop includes a voltage measurement circuit, operatively connected to said
3 phase-locked loop filter, to measure a voltage being output from said phase-locked loop filter; an
4 analog to digital converter, operatively connected to said voltage measurement circuit, to convert
5 the measured voltage into a digital signal; and a controller to cause said programmable charge
6 pump to adjust its output current level based upon a received digital signal from said analog to
7 digital converter.

1 3. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 1,
2 wherein said control loop controls said programmable charge pump to adjust its output current
3 level so that the product of the measured gain and a charge pump current level is kept constant.

1 4. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 2,
2 further comprising:
3 a voltage reference circuit, operatively connected to said programmable charge pump and
4 said analog to digital converter, to generate and apply a same reference voltage to said
5 programmable charge pump and said analog to digital converter based upon changes in a
6 bandgap voltage.

1 5. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 1,
2 further comprising:

3 an integer-N divider operatively connected to an output of said oscillator; and
4 a phase and frequency detector operatively connected between said integer-N divider and
5 said programmable charge pump.

1 6. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 5,
2 wherein said control loop controls said programmable charge circuit to adjust its output current
3 level so that the product of the measured gain and a charge pump current level divided by an
4 average N value, said N value being provided by said integer-N divider, is kept constant.

1 7. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 1,
2 further comprising:

3 an integer-N divider operatively connected to an output of said oscillator;
4 a sigma-delta-modulator operatively connected to said integer-N divider; and
5 a phase and frequency detector operatively connected between said integer-N divider and
6 said programmable charge pump.

1 8. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 7,
2 wherein said control loop controls said programmable charge pump to adjust its output current
3 level so that the product of the measured gain and a charge pump current level divided by an
4 average N value, said N value being provided by said integer-N divider, is kept constant.

1 9. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 1,
2 further comprising:

3 a programmable gain amplifier to receive either a signal from a calibration signal;
4 a comparator for comparing a voltage of an output from said programmable gain
5 amplifier with a voltage necessary to produce a predetermined frequency shift in said oscillator
6 to produce a gain signal; and
7 a gain controller, in response to said gain signal produced by said comparator, to control
8 a gain of said programmable gain amplifier.

1 10. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 9,
2 wherein said gain controller includes a counter and a plurality of resistors, said plurality of
3 resistors being switchable into or out of a circuit connected between an output of said
4 programmable gain amplifier and an input of said programmable gain amplifier.

1 11. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 9,
2 wherein said gain controller controls the gain of said programmable gain amplifier such that a
3 full scale input to said programmable gain amplifier produces said predetermined frequency shift
4 in said oscillator.

1 12. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 1,
2 wherein said phase-locked loop filter includes a capacitor; a charging circuit to pre-charge said
3 capacitor to a voltage of said phase-locked loop filter; and a switch to switch said capacitor into
4 the phase-locked loop filter circuit to effect a phase-locked loop bandwidth.

1 13. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim 1,
2 wherein said phase-locked loop filter includes a dual path having an integrator path and a lead-
3 lag path.

1 14. (Original) The phase-locked loop bandwidth calibration circuit as claimed in claim
2 13, wherein said programmable charge pump provides a first current output level to said
3 integrator path and a second current output level to said lead-lag path.

1 15. (Withdrawn) A phase-locked loop circuit, comprising:
2 a programmable charge pump;
3 a phase-locked loop filter operatively connected to said programmable charge pump; and
4 an oscillator, operatively connected to said phase-locked loop filter, to generate a
5 frequency signal based upon a signal received from said phase-locked loop filter;
6 said programmable charge pump having a resistive value;
7 said phase-locked loop filter having a resistive value;

8 said resistive value of said programmable charge pump being matched to said resistive
9 value of said phase-locked loop filter.

1 16. (Withdrawn) The phase-locked loop circuit as claimed in claim 15, further
2 comprising:

3 a control loop operatively connected to said phase-locked loop filter and said
4 programmable charge pump;

5 said control loop controlling said programmable charge pump to adjust its output current
6 level based on a measured gain of said oscillator.

1 17. (Withdrawn) The phase-locked loop circuit as claimed in claim 16, wherein said
2 control loop includes a voltage measurement circuit, operatively connected to said phase-locked
3 loop filter, to measure a voltage being output from said phase-locked loop filter; an analog to
4 digital converter, operatively connected to said voltage measurement circuit, to convert the
5 measured voltage into a digital signal; and a controller to cause said programmable charge pump
6 to adjust its output current level based upon a received digital signal from said analog to digital
7 converter.

1 18. (Withdrawn) The phase-locked loop circuit as claimed in claim 16, wherein said
2 control loop controls said programmable charge pump to adjust its output current level so that
3 the product of the measured gain and a charge pump current level is kept constant.

1 19. (Withdrawn) The phase-locked loop circuit as claimed in claim 17, further
2 comprising:

3 a voltage reference circuit, operatively connected to said programmable charge pump and
4 said analog to digital converter, to generate and apply a same reference voltage to said
5 programmable charge pump and said analog to digital converter based upon changes in a
6 bandgap voltage.

1 20. (Withdrawn) The phase-locked loop circuit as claimed in claim 16, further
2 comprising:

3 an integer-N divider operatively connected to an output of said oscillator; and

4 a phase and frequency detector operatively connected between said integer-N divider and
5 said programmable charge pump.

1 21. (Withdrawn) The phase-locked loop circuit as claimed in claim 20, wherein said
2 control loop controls said programmable charge circuit to adjust its output current level so that
3 the product of the measured gain and a charge pump current level divided by an average N value,
4 said N value being provided by said integer-N divider, is kept constant.

1 22. (Withdrawn) The phase-locked loop circuit as claimed in claim 16, further
2 comprising:

3 a programmable gain amplifier to receive either a signal from a calibration signal;
4 a comparator for comparing a voltage of an output from said programmable gain
5 amplifier with a voltage necessary to produce a predetermined frequency shift in said oscillator
6 to produce a gain signal; and

7 a gain controller, in response to said gain signal produced by said comparator, to control
8 a gain of said programmable gain amplifier.

1 23. (Withdrawn) The phase-locked loop circuit as claimed in claim 22, wherein said gain
2 controller includes a counter and a plurality of resistors, said plurality of resistors being
3 switchable into or out of a circuit connected between an output of said programmable gain
4 amplifier and an input of said programmable gain amplifier.

1 24. (Withdrawn) The phase-locked loop bandwidth calibration circuit as claimed in claim
2 22, wherein said gain controller controls the gain of said programmable gain amplifier such that
3 a full scale input to said programmable gain amplifier produces said predetermined frequency
4 shift in said oscillator.

1 25. (Withdrawn) The phase-locked loop circuit as claimed in claim 16, wherein said
2 phase-locked loop filter includes a capacitor; a charging circuit to pre-charge said capacitor to a
3 voltage of said phase-locked loop filter; and a switch to switch said capacitor into the phase-
4 locked loop filter circuit to effect a phase-locked loop bandwidth.

1 26. (Withdrawn) The phase-locked loop circuit as claimed in claim 16, wherein said
2 phase-locked loop filter includes a dual path having an integrator path and a lead-lag path.

1 27. (Original) A method of calibrating a phase-locked loop bandwidth, comprising:
2 (a) setting a phase-locked loop at a local oscillator offset;
3 (b) allowing the phase-locked loop to settle;
4 (c) measuring a first gain of a voltage-controlled oscillator located in the phase-locked
5 loop;
6 (d) setting the phase-locked loop to a channel center frequency;
7 (e) allowing the phase-locked loop to settle;
8 (f) measuring a second gain of the voltage-controlled oscillator;
9 (g) determining a difference between the first and second gain measurements; and
10 (h) controlling a programmable charge circuit located in the phase-locked loop to adjust
11 its output current level based on the determined gain difference.

1 28. (Original) The method as claimed in claim 27, wherein the programmable charge
2 circuit adjusts its output current level so that the product of a measured gain and a charge pump
3 current level is kept constant.

1 29. (Withdrawn) A system for processing received radio-frequency signals, comprising:
2 a receiver to receive the radio-frequency signals;
3 a mixing unit to mix down the received radio-frequency signals to baseband;
4 a frequency synthesizer to generate signals used by said mixing unit in mixing down the
5 received radio-frequency signals to baseband;
6 a filtering unit to lowpass filter the baseband radio-frequency signals; and
7 a RC calibration unit to determine R and C values of said filtering unit so as to calibrate
8 pole & zero frequencies of said filtering unit;
9 said frequency synthesizer including a phase-locked loop circuit having a programmable
10 charge pump, a phase-locked loop filter operatively connected to said programmable charge

11 pump, and an oscillator, operatively connected to said phase-locked loop filter, to generate a
12 frequency signal based upon a signal received from said phase-locked loop filter;
13 said RC calibration unit using said determined R and C values to calibrate pole & zero
14 frequencies of said phase-locked loop filter.

1 30. (Withdrawn) The system as claimed in claim 29, further comprising:
2 a control loop operatively connected to said phase-locked loop filter and said
3 programmable charge pump;
4 said control loop controlling said programmable charge pump to adjust its output current
5 level based on a measured gain of said oscillator.

1 31. (Withdrawn) The system as claimed in claim 30, wherein said control loop includes a
2 voltage measurement circuit, operatively connected to said phase-locked loop filter, to measure a
3 voltage being output from said phase-locked loop filter; an analog to digital converter,
4 operatively connected to said voltage measurement circuit, to convert the measured voltage into
5 a digital signal; and a controller to cause said programmable charge pump to adjust its output
6 current level based upon a received digital signal from said analog to digital converter.

1 32. (Withdrawn) The system as claimed in claim 30, wherein said control loop controls
2 said programmable charge pump to adjust its output current level so that the product of the
3 measured gain and a charge pump current level is kept constant.

1 33. (Withdrawn) The system as claimed in claim 31, further comprising:
2 a voltage reference circuit, operatively connected to said programmable charge pump and
3 said analog to digital converter, to generate and apply a same reference voltage to said
4 programmable charge pump and said analog to digital converter based upon changes in a
5 bandgap voltage.

1 34. (Withdrawn) The system as claimed in claim 30, further comprising:
2 an integer-N divider operatively connected to an output of said oscillator; and
3 a phase and frequency detector operatively connected between said integer-N divider and
4 said programmable charge pump.

1 35. (Withdrawn) The system as claimed in claim 30, further comprising:
2 a programmable gain amplifier to receive either a signal from a calibration signal;
3 a comparator for comparing a voltage of an output from said programmable gain
4 amplifier with a voltage necessary to produce a predetermined frequency shift in said oscillator
5 to produce a gain signal; and
6 a gain controller, in response to said gain signal produced by said comparator, to control
7 a gain of said programmable gain amplifier.

1 36. (Withdrawn) The system as claimed in claim 30, wherein said phase-locked loop
2 filter includes a capacitor; a charging circuit to pre-charge said capacitor to a voltage of said
3 phase-locked loop filter; and a switch to switch said capacitor into the phase-locked loop filter
4 circuit to effect a phase-locked loop bandwidth.

1 37. (Withdrawn) The system as claimed in claim 30, wherein said phase-locked loop
2 filter includes a dual path having an integrator path and a lead-lag path.

1 38. (Withdrawn) The system as claimed in claim 29, wherein said programmable charge
2 pump has a resistive value; said phase-locked loop filter has a resistive value; and said resistive
3 value of said programmable charge pump is matched to said resistive value of said phase-locked
4 loop filter.

1 39. (Withdrawn) The system as claimed in claim 30, wherein said programmable charge
2 pump has a resistive value; said phase-locked loop filter has a resistive value; and said resistive
3 value of said programmable charge pump is matched to said resistive value of said phase-locked
4 loop filter.